Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) A semiconductor memory device comprising testmode circuitry, adapted to maintain a pair of bitlines coupled to a memory cell within the device to the same logic state during operation of the testmode circuitry by forwarding a direct current from a voltage source to each of the pair of bitlines through a path that comprises a respective local interconnect structure, wherein the bitlines are not maintained at the logic state during ordinary operation of the device.

2. (Canceled)

3. (Original) The semiconductor memory device as recited in claim ~~2~~ 1, further comprising a user-determined voltage from the voltage source.

4. (Original) The semiconductor memory device as recited in claim ~~2~~ 1, wherein the direct currents flow for a user-determined time.

5. (Canceled)

6. (Original) The semiconductor memory device as recited in claim ~~5~~ 1, wherein each of the local interconnect structures comprises at least one contact through which the respective direct current passes when the bitlines are at the same logic state.

7. (Original) The semiconductor memory device as recited in claim 1, wherein the testmode circuitry is further adapted to force the pair of bitlines to circuit ground.

8. (Original) The semiconductor memory device as recited in claim 1, wherein the testmode circuitry is further adapted to hold the bitlines at the same logic state for a user-determined length of time.

9. (Currently Amended) A system for testing a semiconductor memory device, said system comprising testmode circuitry within the semiconductor memory device adapted to maintain a pair of bitlines coupled to a memory cell within the memory device to the same logic state, wherein the bitlines are not maintained at the logic state during ordinary operation of the device.